LOW POWER, AREA-EFFICIENT CIRCUIT TO PROVIDE CLOCK SYNCHRONIZATION

ABSTRACT

A clock signal generator, which requires no clock selection pin includes a multiplexer to which external and internal clocks are applied. The external clock is further coupled directly and via an inverting delay to a logic circuit, the output of which controls a switching device connected across a capacitor. The capacitor is coupled to a current source and to a comparator that is coupled to a reference voltage. The comparator output serves as the select control for the multiplexer. The switching device repeatedly discharges the capacitor in response to the external clock signal, but otherwise allows the capacitor to be charged by the current source. The external clock signal is coupled to the output of the multiplexer, as long as the capacitor is repeatedly discharged by the external clock signal at a frequency sufficient to maintain the voltage across the capacitor less than the reference voltage.